

Abstract of the Disclosure

A preferred exemplary embodiment of the current invention concerns a memory testing process, wherein circuitry is provided to allow on-chip comparison of stored data and expected data. The on-chip comparison allows the tester to transmit in a parallel manner the expected data to a plurality of chips. In a preferred embodiment, at most one address -- and only the column address -- corresponding to a failed memory cell is stored in an on-chip address register at one time, with each earlier failed addresses being cleared from the register in favor of a subsequent failed address. Another bit -- the "fail flag" bit -- is stored in the address register to indicate that a failure has occurred. If the fail flag is present in a chip, that chip is repaired by electrically associating the column address with redundant memory cells rather than the original memory cells. Data concerning available redundant cells may be stored in at least one on-chip redundancy register. Additional circuitry is preferably provided to allow early switching of input signals from a first configuration directed to blow a first anti-fuse to a second configuration directed to blow a second anti-fuse, yet still allow complete blowing of the first anti-fuse. After repair, the chip's registers may be cleared and testing may continue. It is preferred that the address register and related logic circuitry be configured to avoid storing an address that is already associated with a redundant cell, even though that redundant cell has failed.